TECHNICAL REPORT

TITLE : **Technical Report on Timing Filter Amplifier and Constant Fraction Discriminator (TFA + CFD)**

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(TFA + CFD)

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on
Timing Filter Amplifier and
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Abstract

As a part of on going Nuclear Electronics development for INGA project, we have successfully developed a compact Timing Filter Amplifier (TFA) and Constant Fraction Discriminator (CFD) for Clover array with SMD technology. It essentially consists of a gain stage, RC shaping with P/Z correction, Robinson diode base line restorer (BLR) correction and coaxial cable driver. It has the option for remote Pole-Zero (P/Z) adjustment.

Various prototypes have been tested with HPGe and scintillator (ACS) detectors. The principle of operation of various circuit blocks are explained along with representative test point signals. Assembly and troubleshooting procedures are given. Possible improvements are also suggested.

Acknowledgment

SPECIFICATIONS

TIMING FILTER AMPILIFIER

INPUT IMPEDANCE	50 / 100 ohms.
GAIN(fixed)*	~11
	The input of -200mV/MeV is expected from Preamplifier.
OUTPUT AMPLITUDE	0 to ±2.5V into 50 ohm cable and load.
	Zo : <1 ohm
RISE TIME	Better than 10 nS. With no additional integration across dynamic range.
STABILITY (DC)	Twin diode base line restorer used.
P/Z ADJUSTMENT*	P/Z internally corrected for 50μS (±5%) decay time.
DIFFERENTIATION	200nS (C1 X R12)
INTEGRATION	none. (R4 X Cx)

Note: * **For ACS, the P/Z network is wired for 400nS internally to match the decay time of BGO phosphor.**

CONSTANT FRACTION DISCRIMINATOR

INPUT SIGNAL	Negative pulses accepted upto -5V
DISCRIMINATOR RANGE	+60mV to -200mV
(LLTH)	Front panel adjusted.
LLTH MONitor	Measures x10 of actual LLTH set value.
DELAY	Internal, Zo = 100 0hm, 25nSec Fixed.
FRACTION RATIO	x 0.3
WALK ADJUST	Front panel control for exact zero-cross voltage.
WALK MONitor	Front panel LEMO connector for monitoring Zero cross signal.
DEAD TIME	2 μS (Clover only)
OUTPUTS	ECL DIFFERENTIAL 2 μS
	ECL DIFFERENTIAL 50 nS
	FAST NIM (2 nos.) 50 nS (Clover)
	FAST NIM (2 nos.) 500 nS (ACS)
IMPEDANCE	100 ohm DIFFERENTIAL ECL
	50 ohm FAST NIM
OTHERS	SRT/CFD selection (Jumper on board)
DIMENSION & WEIGHT	(WXHXL) 1.5" x 4" x 0.5", 50 grams

Note: For ACS, the same type CFD daughter card is utilized without any dead time.

Introduction

Timing Filter Amplifier: The signal from HPGe detectors through preamplifier is not optimum from achieving good timing resolution. Before applying the signal to CFD, the signal need an amplification to a reasonable level, as well as some additional signal shaping so as to extract best timing resolution. A timing filter amplifier (TFA) consists of Pole-Zero (P/Z) correction network, RC differentiator, Integrator, Robinson base Line restorer and buffer. The gain and buffer stages are made of wide band operational amplifiers with high slew rate. The P/Z range, differentiation, Integration time constants, gain settings are custom selected as per system requirements. The functional block diagram is shown.

Constant Fraction Discriminator: A typical second generation CFD technique with amplitude rise time correction (ARC) and slow rise time reject (SRT) is adopted to suit with the large volume HPGe detector output. The signal from TFA is fed to a low level threshold (LLTH) discriminator and Constant Fraction (CF) circuits simultaneously. When the input exceeds the set LLTH reference level, the discriminator generates a logic level t_{LE}. The LLTH discriminator provides energy selection across a specified range. Further, in CF section, the input signal is delayed and a fraction (F)of undelayed signal are applied to fast comparator inputs to form a CF timing signal t_{CF} . The delay is chosen to make optimum fraction correspond to the leading edge of the delayed pulse establishing a line up with peak amplitude of attenuated pulse. The timing signal t_{CF} acts as a time marker at the optimum height of the input pulse and becomes independent of the pulse amplitude variations. Usually $t_{LE} > t_{CF}$. Due to considerable rise time variations exist in the output of a HPGe detector, usually ARC technique is adopted. Here

$$T_{delay} << T_{rise},$$

so that cross over occurs at the fast rising part of the signals. Therefore,

$$t_{CF} = Td / (1-f)$$

with a condition that **$T_{delay} << T_{rise}(min) (1-f).$**

Slow rise Time reject (SRT)

The CFD can be operated with SRT selection as well. This is required to evaluate the CFD and LLTH signals in order to reject the slow ones. For a very slow signal, the LLTH signal would come subsequent to the CFD timing signal, and thereby causing WALK and related degradation in timing resolution. SRT selection would help block such slow signal. This helps in improving the timing resolution at the cost of counting efficiency.

Principle of Operations

TFA: The TIME_IN signal from Preamplifier is terminated on input resistor 100 ohms. This is followed by a passive Pole-Zero (P/Z) correction, designed to handle 50 µS decay time signal. The P/Z_COMP signal from corresponding Spectroscopy amplifier is used to fine control the P/Z correction. The differentiation is of 200 nS is implemented with R12, C1. No additional integration is implemented in this scheme. The signal is fed to a High speed Current Feedback Amplifier (CFA) type AD8011AR and amplified suitably. The expected high count rate may paralyse the system due to base-line shift and DC offset in amplification stage. A twin-diode Robinson restorer circuit is adopted for simplicity. A capacitor C2, is used for DC blocking, matched SCHOTTKY diode is biased with 0.1mA current through high ohmic resistor to act as a switch. The final stage is a wide band driver amplifier with high slew rate. The power supply (6V) lines are suitably ac coupled to avoid spurious oscillations. High quality resistors, capacitors in SMT are used for high density as well as high frequency operations.

CFD: The CFD is assembled in the same PCB as TFA but with isolated ground. The supply lines are isolated with 1A Silicon diodes and DC coupled appropriately with high and low value capacitors.

The input impedance of CFD is kept at 100 ohms and it accepts negative signals from TFA. The upper part of Ultra fast Comparators (U4A) is used to generate energy dependent timing signal (t_{LLTH}). The threshold for this comparator is generated from a temperature compensated low power voltage regulator LM336 (2.5V) and associated circuit. The LLTH level can be adjusted from 60mV to -200mV through front panel potentiometer or through remote DAC.

The CF is implemented at the inputs of another comparator (U4B). The fraction is chosen as 0.3 and implemented with high precision resistors. The input signal is delayed with lumped constant fixed delay line module (25nS, 100 ohms). The attenuated and delayed signal are fed to this comparator simultaneously to generate Constant Fraction (CF) logic signal. The "WALK" adjustment is provided through front panel potentiometer along with a monitoring point (WALK_MON). The LLTH signal from U4A is used as a arm signal for CF output in a ECL AND gate U5C and usually t_{LLTH}> t_{CF}. In a large volume detector, the rise time variation is high and very slow signal rejection is imperative to improve the timing resolution with accepting somewhat poor count rate efficiency. For a very slow signal t_{LLTH}<t_{CF}. The Monoshot circuit output is blocked for a delayed LLTH signal using SRT option. Resulting true timing signal is then used to generate a fixed width 2μS dead time where any further Z/C signals are blocked for this time duration. The signal is used to generate another Mono-shot to generate fixed with (50nS) CFD output. These ECL signals are level converted (Q1-Q4) to generate F_NIM level signals across 50 ohm. The intermediate logic (ECL) level signals at monoshots are accessed for easy implementation of Anti_Coincidence Logic.

Assembly Procedure

The currently available PCB (TFA+CFD MAY_2K2) is of glass epoxy, double sided with 0.7mm drill PTH having dimension of 4" x 1.5" with all above features. All developed prototypes have common PCB foot prints in order to use them conveniently.

It is recommended to have solder mask and silk screen printed on both sides for easy assembly as well to protect it from solder bridges etc.,. Use of 0.8mm sharp solder tip, IC solder tips are recommended in order to solder narrowly spaced SMT devices. SMT devices shall be picked only by fine quality tweezers. While soldering a magnifier x5 (large) and x12 (eye piece) is used to assure the soldering. It is essential to use solder cleaning liquid with cotton swab to remove dust attracting solder paste.

The PCB shall be checked with magnifiers and multimeter for any unwanted connections and PTHs. Then components shall be soldered in a orderly manner, to start with all low profile chip resistors and capacitors. It is essential to check the impedance between various nodes after soldering resistors, capacitors and inductors. Active components like diodes, transistors and ICS are soldered thereafter. At last tantalum capacitors, connectors, jumpers and any non-SMT devices. All PCBs shall be marked distinctly with unique number for any future references.

Further Improvements

In order to make the TFA +CFD card further versatile, we intend to incorporate

Auto WALK adjustment: This would reduce complication of adjusting WALK and simple front panel connections.

Implementation of ECL monoshot with Ultra fast comparators: This would avoid usage of MC10198 an obsolete power hungry chip and will facilitate remote control of timing durations. In order to use with standard CAMAC frame, it is suggested to reduce the height of the PCB as well as implementing in multilayer (4 layers) for timing resolution.

References

The following references were proven to be very useful to design and test TFA+CFD module.

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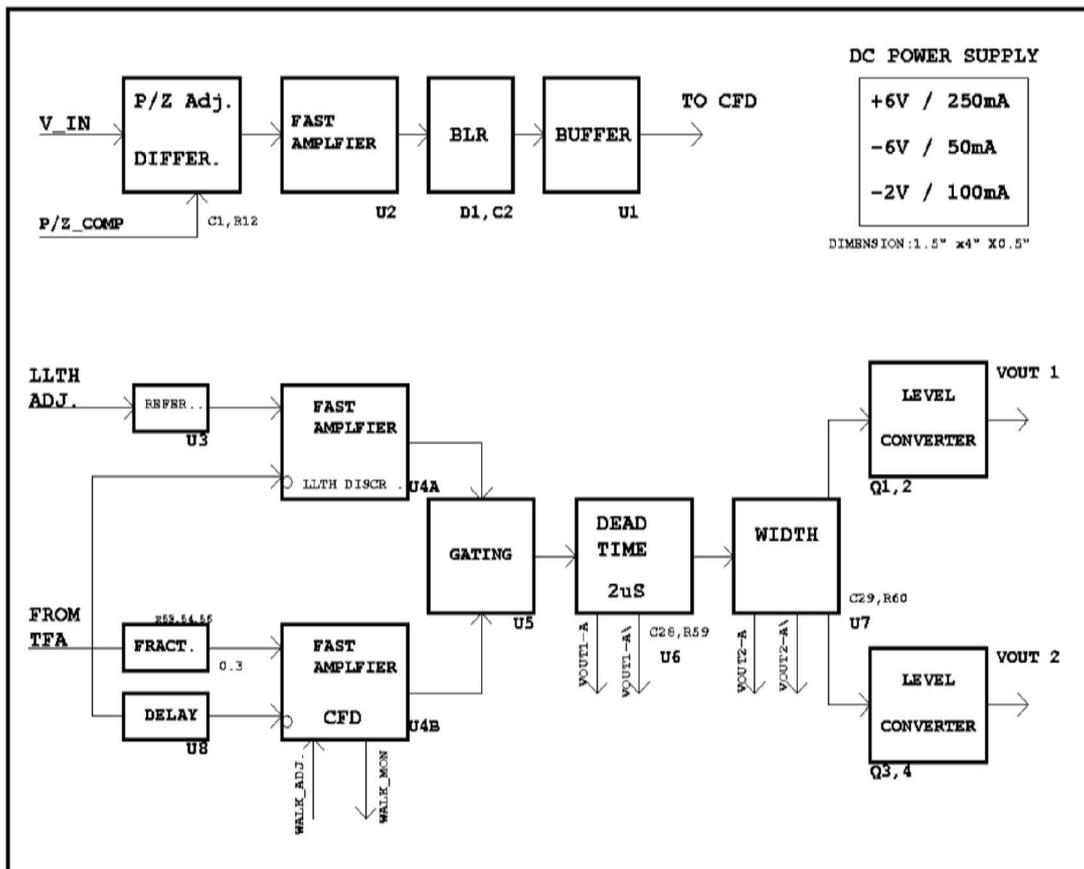
Fig: Block Diagram

Fig: TFA + CFD daughter Card (ACS type shown here)
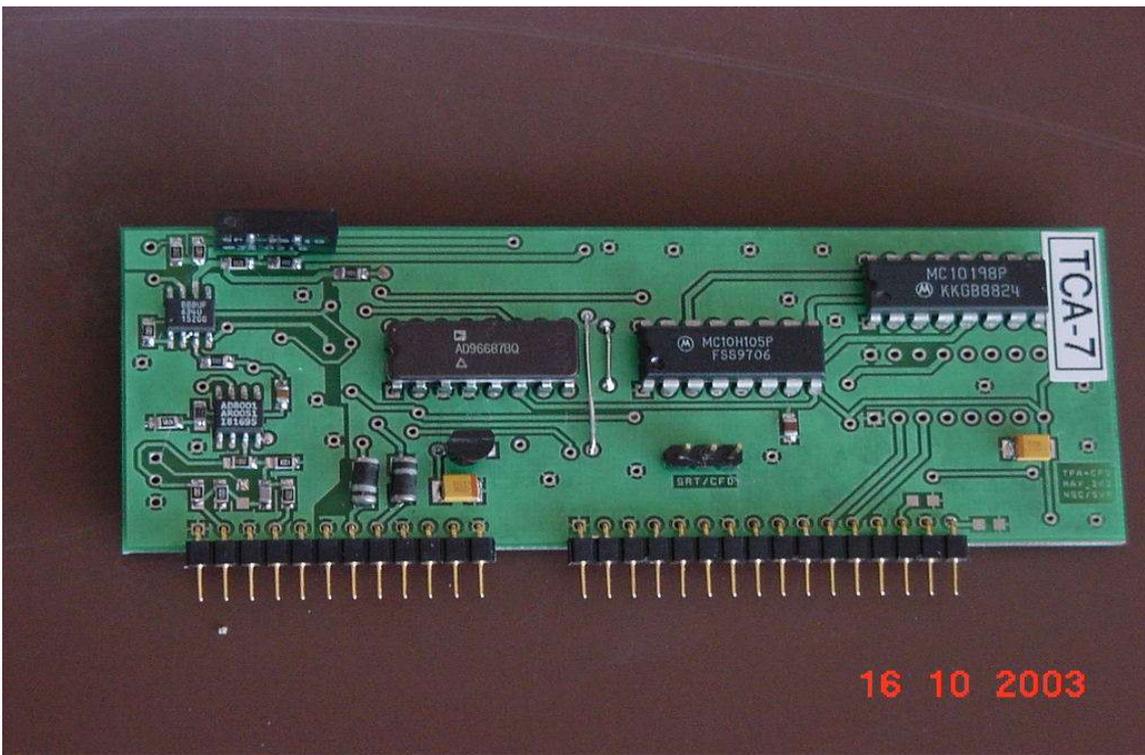
Fig: Typical ACS TFA Monitor and CFD outputs.